--ABSTRACT OF THE DISCLOSURE

A method for fabricating an electronic component with a self-aligned source, drain and gate. The method includes forming a dummy gate on a silicon substrate, in which the dummy gate defines a position for a channel of the component. The method also includes at least one implantation of doping impurities in the substrate, to form a source and a drain on either side of the channel, using the dummy gate as an implanting mask, superficial, self-aligned siliciding of the source and drain, depositing at least one contact metal layer having a total thickness greater than a height of the dummy gate, polishing the at least one contact metal layer stopping at the dummy gate, and replacing the dummy gate by at least one final gate separated from the substrate by a gate insulating layer, and electrically insulated from the source and drain. Further, depositing the at least one contact metal layer includes depositing a first metal layer and, above the first metal layer, a second metal layer having a greater mechanical resistance to polishing than the first metal layer. In addition, a thickness of the first metal layer is less than the height of the dummy gate, and a total thickness of the first and second layers is greater than the height of the dummy gate. Further, the first metal is chosen from among tungsten and titanium, and the second metal is chosen from among TaN, Ta and TiN.--

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-11 are pending in the present application. Claims 1-10 have been amended and Claim 11 has been added by the present amendment.